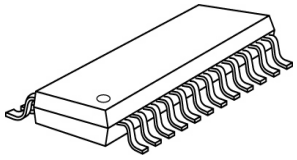
16-Channel PWM Constant Current LED Driver for 1:32 Time-Multiplexing Applications

Features

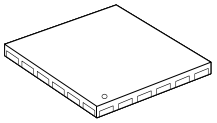
- 3V-5.5V supply voltage
- 16 constant current output channels
- Constant output current range:
  - 0.5~20mA @ 5V supply voltage
  - 0.5~15mA @ 3.3V supply voltage
- Excellent output current accuracy:
  Between channels:：<±2.5%(Max.)
  Between ICs: <±3%(Max.)
- Digital Power-On-Reset
- Built-in 16K-bit SRAM to support time-multiplexing for 1 ~ 32 scans
- 14-bit /13-bit color depth PWM control to improve visual refresh rate
- 6-bit current gain，12.5%~100%
- LED failure isolation
  -LED failure induced cross elimination
- Compulsory LED open detection
- Integrating ghost elimination circuit
- Improvement of high contrast interference
- GCLK multiplier technology
- Support double refresh mode
- Maximum data clock frequency: 30MHz@VDD=5V
- Maximum gray-scale clock frequency: 33MHz @VDD=5V

Shrink SOP



GP: SSOP24L-150-0.64

Quad Flat No-leads



GFN: QFN24L-4x4-0.5

Product Description

MBI5253 is designed for LED video applications using internal Pulse Width Modulation (PWM) control with selectable 14-bit / 13-bit color depth. MBI5253 features a 16-bit shift register which converts serial input data into each pixel's gray scale of the output port. Sixteen regulated current ports are designed to provide uniform and constant current sinks for driving LEDs with a wide range of V_F variations. The output current can be preset through an external resistor. The innovative architecture with embedded SRAM is designed to support up to 1:32 time-multiplexing applications. Users only need to send the whole frame data once and to store in the embedded SRAM of the LED driver, instead of sending every time when the scan line is changed. It helps to save the data bandwidth and to achieve high grayscale with very low data clock rate. With scan-type Scrambled-PWM (S-PWM) technology, MBI5253 enhances PWM by scrambling the "on" time of each scan line into several "on" periods and sequentially drives each scan line for a short "on" period. The enhancement equivalently increases the visual refresh rate of scan-type LED displays. In addition, the innovative GCLK multiplier technique doubles visual refresh rate.

MBI5253 drives the corresponding LEDs to the brightness specified by image data. With MBI5253, all output channels can be built with 14-bit color depth. When building a 14-bit color depth video, S-PWM technology reduces the flickers and improves the image fidelity.

Floor 6-4, No.18, Pu-Ting Rd., Hsinchu, Taiwan 30072, ROC.
TEL: +886-3-579-0068, FAX: +886-3-579-7534 E-mail: info@mblock.com.tw

Through compulsory error detection, MBI5253 detects individual LED for open-circuit errors without extra components. MBI5253 equipped an innovative cross elimination function, and it solves the cross phenomenon induced by failure LEDs. Besides, integrated ghost elimination and high contrast interference circuit eases the ghost problems and improve image contrast.

Block Diagram

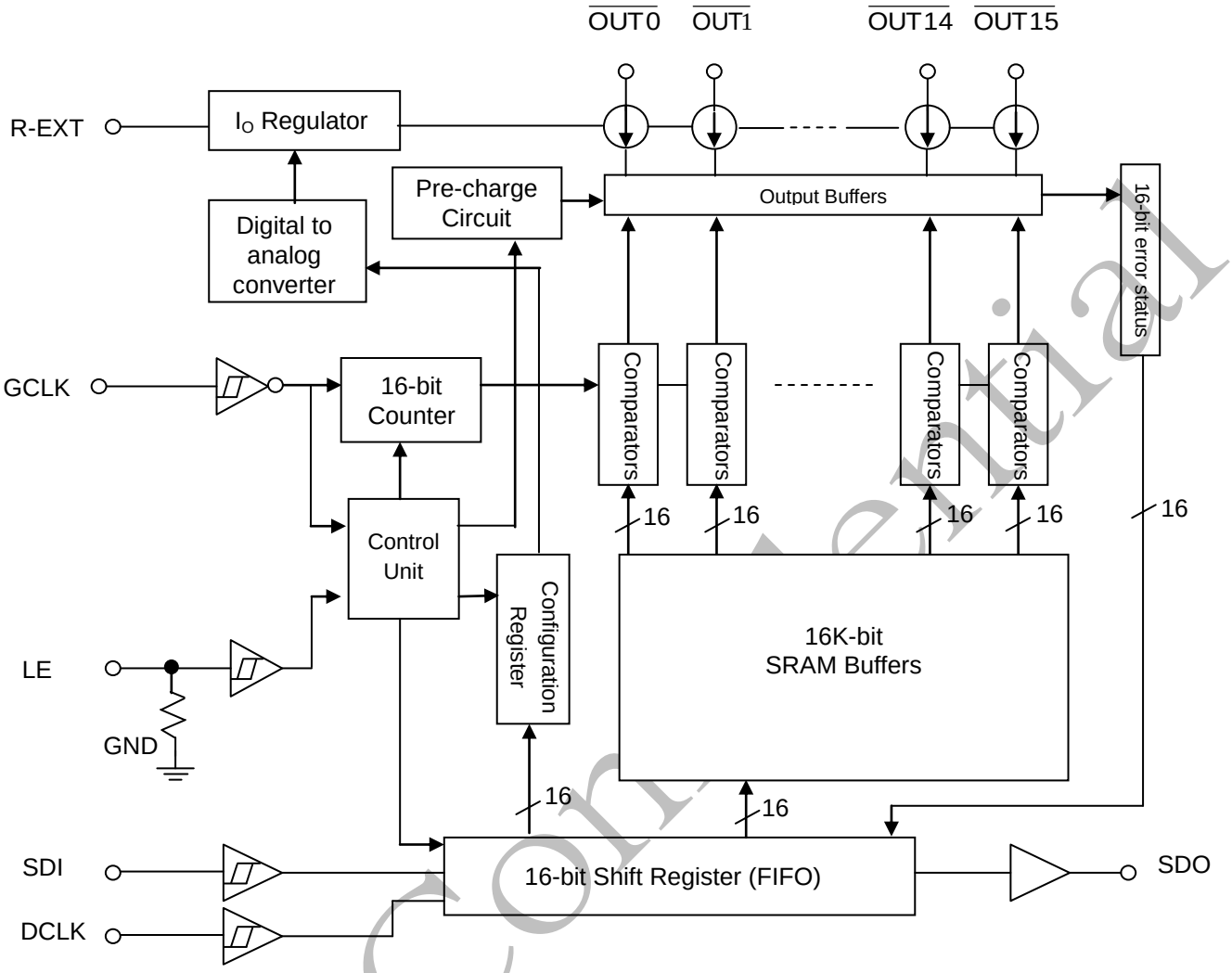
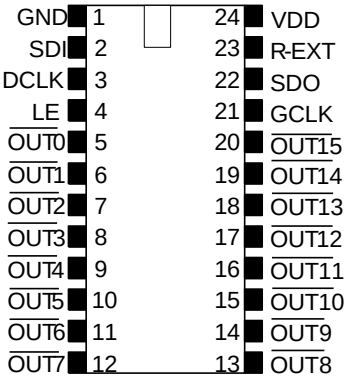
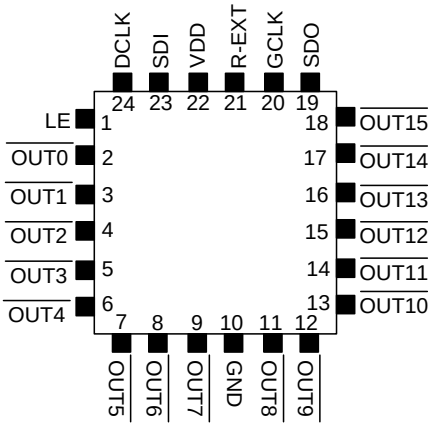


Figure 1

Pin Configuration



MBI5253GP



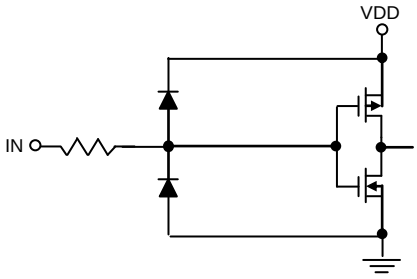
MBI5253GFN

Terminal Description

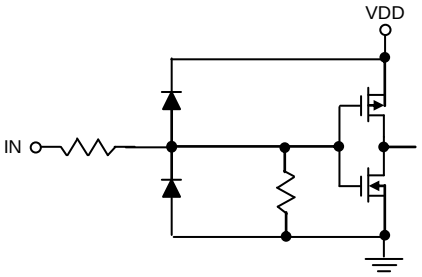
Pin Name	Function
GND	Ground terminal for control logic and current sink
SDI	Serial-data input to the shift register
DCLK	Clock input terminal used to shift data on rising edge and carries command information when LE is asserted.
LE	Data strobe terminal and controlling command with DCLK
$\overline{OUT0}$~$\overline{OUT15}$	Constant current output terminals
GCLK	Gray scale clock terminal Clock input for gray scale. The gray scale display is counted by gray scale clock compared with input data.
SDO	Serial-data output to the receiver-end SDI of next LED driver
R-EXT	Input terminal used to connect an external resistor for setting up output current for all output channels
VDD	3.3V/5V supply voltage terminal

Equivalent Circuits of Inputs and Outputs

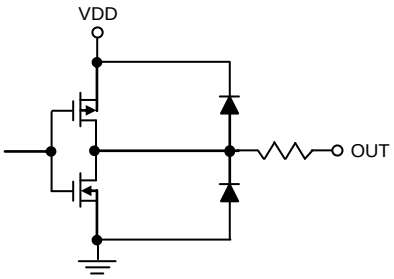
GCLK, DCLK, SDI terminal



LE Terminal



SDO Terminal



Maximum Rating

Characteristic		Symbol	Rating	Unit
Supply Voltage		V_{DD}	0~5.5	V
Input Pin Voltage (SDI, DCLK, GCLK, LE)		V_{IN}	-0.4~V_{DD}+0.4	V
Sustaining Voltage at OUT Port		V_{DS}	-0.5 ~ +7	V
Output Current		I_{OUT}	+22	mA
GND Terminal Current		I_{GND}	360	mA
Power Dissipation (On 4 Layer PCB, Ta=25°C)*	GP Type	P_D	1.79	W
	GFN Type		3.12	
Thermal Resistance (On 4 Layer PCB, Ta=25°C)*	GP Type	$R_{th(j-a)}$	69.5	°C/W
	GFN Type		40.01	
Junction Temperature		$T_{j,max}$	150**	°C
Operating Ambient Temperature		T_{opr}	-40~+85	°C
Storage Temperature		T_{stg}	-55~+150	°C
ESD Rating	HBM (MIL-STD-883G Method 3015.7, Human Body Mode)	HBM	Class 3A (5KV)	-
	MM (JEDEC EIA/JESD22-A115, Machine Mode)	MM	Class M4 (≧400V)	-

*The PCB size is 76.2mm*114.3mm in simulation. Please refer to JEDEC JESD51.

** Operation at the maximum rating for extended periods may reduce the device reliability; therefore, the suggested junction temperature of the device is under 125°C.

Note: The performance of thermal dissipation is strongly related to the size of thermal pad, thickness and layer numbers of the PCB. The empirical thermal resistance may be different from simulative value. User should plan for expected thermal dissipation performance by selecting package and arranging layout of the PCB to maximize the capability.

Electrical Characteristics (V_{DD}=5.0V, Ta=25˚C)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		4.5	5.0	5.5	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUT0}$~ $\overline{OUT15}$		-	-	7.0	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		0.5	-	20	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	Ta=-40~85ºC		0.7xV_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	Ta=-40~85ºC		GND	-	0.3xV_{DD}	V
Start Up Voltage		V_{STUP}				2.7		V
UVLO Voltage		V_{UVLO}				2.5		V
Output Leakage Current		I_{OH}	V_{DS}=5.4V		-	-	0.5	μA
Output Voltage	SDO	V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
		V_{OH}	I_{OH}=-1.0mA		4.6	-	-	V
Current Skew (Channel)		dI_{OUT1}	I_{OUT}=0.5mA V_{DS}=1.0V	R_{ext}=28.8kΩ	-	±1.5	±2.5	%
Current Skew (IC)		dI_{OUT2}	I_{OUT}=0.5mA V_{DS}=1.0V	R_{ext}=28.8kΩ	-	±1.5	±3	%
Output Current vs. Output Voltage Regulation*		%/dV_{DS}	V_{DS} within 1.0V and 3.0V,		-	±0.1	±0.3	% / V
Output Current vs. Supply Voltage Regulation*		%/dV_{DD}	V_{DD} within 4.5V and 5.5V		-	±1.0	±2.0	% / V
Pull-down Resistor		R_{IN}(down)	LE			100		KΩ
Supply Current (DCLK=GCLK =0Hz)	"Off"	I_{DD}(off) 1	R_{ext}=Open, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off			3.70	4.20	mA
		I_{DD}(off) 2	R_{ext}=28.8kΩ , $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off			3.94	4.94	mA
		I_{DD}(off) 3	R_{ext}=1.4kΩ, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off			6.05	7.05	mA
Supply Current (GCLK=20Hz)	"On"	I_{DD}(on) 2	R_{ext}=28.8kΩ , $\overline{OUT0}$ ~ $\overline{OUT15}$ =ON			4.63	5.63	mA
		I_{DD}(on) 3	R_{ext}=1.4kΩ, $\overline{OUT0}$ ~ $\overline{OUT15}$ =ON			6.81	7.81	mA

*One channel on.

Electrical Characteristics (V_{DD}=4.2V, Ta=25˚C)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		3.8	4.2	4.6	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUT0}$~ $\overline{OUT15}$		-	-	7.0	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		0.5	-	20	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	Ta=-40~85ºC		0.7xV_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	Ta=-40~85ºC		GND	-	0.3xV_{DD}	V
Start Up Voltage		V_{STUP}				2.7		V
UVLO Voltage		V_{UVLO}				2.5		V
Output Leakage Current		I_{OH}	V_{DS}=4.6V		-	-	0.5	μA
Output Voltage	SDO	V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
		V_{OH}	I_{OH}=-1.0mA		3.8	-	-	V
Current Skew (Channel)		dI_{OUT1}	I_{OUT}=0.5mA V_{DS}=1.0V	R_{ext}=28.8kΩ	-	±1.5	±2.5	%
Current Skew (IC)		dI_{OUT2}	I_{OUT}=0.5mA V_{DS}=1.0V	R_{ext}=28.8kΩ	-	±1.5	±3	%
Output Current vs. Output Voltage Regulation*		%/dV_{DS}	V_{DS} within 1.0V and 3.0V,		-	±0.1	±0.3	% / V
Output Current vs. Supply Voltage Regulation*		%/dV_{DD}	V_{DD} within 4.5V and 5.5V		-	±1.0	±2.0	% / V
Pull-down Resistor		R_{IN}(down)	LE			100		KΩ
Supply Current (DCLK=GCLK =0Hz)	"Off"	I_{DD}(off) 1	R_{ext}=Open, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off			3.31	3.81	mA
		I_{DD}(off) 2	R_{ext}=28.8kΩ , $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off			3.49	4.49	mA
		I_{DD}(off) 3	R_{ext}=1.4kΩ, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off			5.59	6.59	mA
Supply Current (GCLK=20Hz)	"On"	I_{DD}(on) 2	R_{ext}=28.8kΩ , $\overline{OUT0}$ ~ $\overline{OUT15}$ =ON			4.46	5.46	mA
		I_{DD}(on) 3	R_{ext}=1.4kΩ, $\overline{OUT0}$ ~ $\overline{OUT15}$ =ON			6.63	7.63	mA

*One channel on

Electrical Characteristics (V_{DD}=3.3V, Ta=25˚C)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		3.0	3.3	3.6	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUT0}$~ $\overline{OUT15}$		-	-	7.0	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		0.5	-	10	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	Ta=-40~85ºC		0.7xV_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	Ta=-40~85ºC		GND	-	0.3xV_{DD}	V
Start Up Voltage		V_{STUP}				2.7		V
UVLO Voltage		V_{UVLO}				2.5		V
Output Leakage Current		I_{OH}	V_{DS}=3.7V		-	-	0.5	μA
Output Voltage	SDO	V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
		V_{OH}	I_{OH}=-1.0mA		2.9	-	-	V
Current Skew (Channel)		dI_{OUT}	I_{OUT}=0.5mA V_{DS}=1.0V	R_{ext}=28.8kΩ	-	±1.5	±2.5	%
Current Skew (IC)		dI_{OUT2}	I_{OUT}=0.5mA V_{DS}=1.0V	R_{ext}=28.8kΩ	-	±1.5	±3	%
Output Current vs. Output Voltage Regulation*		%/dV_{DS}	V_{DS} within 1.0V and 3.0V,		-	±0.1	±0.3	% / V
Output Current vs. Supply Voltage Regulation*		%/dV_{DD}	V_{DD} within 3.0V and 3.6V		-	±1.0	±2.0	% / V
Pull-down Resistor		R_{IN}(down)	LE			100		KΩ
Supply Current (DCLK=GCLK =0Hz)	"Off"	I_{DD}(off) 1	R_{ext}=Open, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off			3.26	3.76	mA
		I_{DD}(off) 2	R_{ext}=28.8kΩ , $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off			3.43	4.43	
		I_{DD}(off) 3	R_{ext}=1.4kΩ, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off			4.50	5.50	
Supply Current (GCLK=20MHz)	"On"	I_{DD}(on) 2	R_{ext}=28.8kΩ , $\overline{OUT0}$ ~ $\overline{OUT15}$ =ON			4.28	5.28	
		I_{DD}(on) 3	R_{ext}=1.4kΩ, $\overline{OUT0}$ ~ $\overline{OUT15}$ =ON			6.41	7.41	

*One channel on.

Test Circuit for Electrical Characteristics

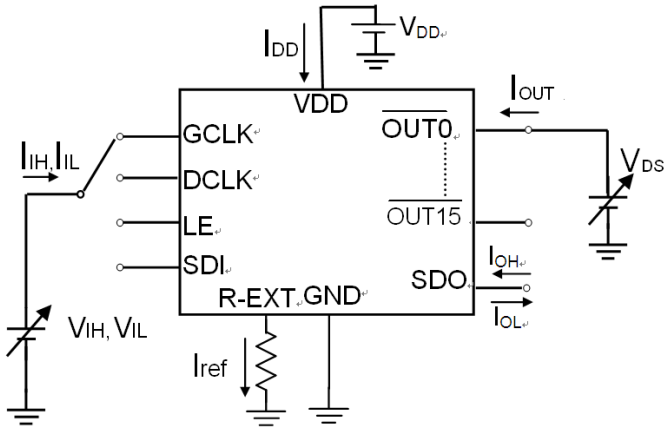


Figure 2

Switching Characteristics (V_{DD}=5.0V, Ta=25°C)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Setup Time	SDI - DCLK↑	t_{SU0}	V_{DD}=5.0V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=1.4kΩ V_{DS}=1V R_L=300Ω C_L=10pF C_1=100nF C_2=10μF C_{SDO}=10pF V_{LED}=4.0V	5	-	-	ns
	LE↑ – DCLK↑	t_{SU1}		8	-	-	ns
	LE↓(vsync/swrst) – GCLK	t_{SU2}		1200			ns
	LE↓ – DCLK↑	tsu3***		50			ns
Hold Time	DCLK↑ - SDI	t_{H0}		6	-	-	ns
	DCLK↑ - LE	t_{H1}		8	-	-	ns
	GCLK – LE↓(vsync/swrst)	t_{H2}		300			ns
Propagation Delay Time	DCLK – SDO	t_{PD0}		-	22	25	ns
	GCLK – $\overline{OUT2n}$*	t_{PD1}		-	35	-	ns
	LE – SDO	t_{PD2}***		-	30	40	ns
Pulse Width	LE	$t_{W(LE)}$		15			ns
Command to command		tcc		50	-	-	ns
Data Clock Frequency		F_{DCLK}		-	-	30	MHz
Gray Scale Clock Frequency		F_{GCLK}		-	-	33	MHz
Gray Scale Clock Frequency (The function of GCLK doubling is enabled)		F_{GCLK}		-	-	16.6	MHz
Min Clock(GCLK/DCLK) pulse width****		$t_{W(CLK)}$		12	-	-	Ns
Ratio of (GCLK freq)/(DCLK freq)		$R_{(GCLK/DCLK)}$		20	-	-	%
Compulsory error detection operation time***		t_{ERR-C}		700	-	-	ns
Output Rise Time of Output Ports		t_{OR}			15	25	ns
Output Fall Time of Output Ports		t_{OF}			15	25	ns
Dead time positive level		tdth		300			ns
Dead time negative level		tdtl		1200			ns

*Output waveforms have good uniformity among channels.

** Refer to the Timing Waveform, where n=0, 1, 2, 3, 4, 5, 6, 7.

***In timing of "configuration read", the next DCLK rising edge should be t_{PD2} after LE's falling edge.

****The Gray Scale Clock period must be 50% duty cycle when the function of GCLK multiplier is enabled.

*****Users have to leave more time than the maximum error detection time for the error detection.

Switching Characteristics (V_{DD}=4.2V, Ta=25°C)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Setup Time	SDI - DCLK↑	t_{SU0}	V_{DD}=4.2V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=1.4kΩ V_{DS}=1V R_L=300Ω C_L=10pF C_1=100nF C_2=10μF C_{SDO}=10pF V_{LED}=4.0V	6	-	-	ns
	LE↑ – DCLK↑	t_{SU1}		9	-	-	ns
	LE↓(vsync/swrst) – GCLK	t_{SU2}		1200			ns
	LE↓ – DCLK↑	tsu3***		51			ns
Hold Time	DCLK↑ - SDI	t_{H0}		7	-	-	ns
	DCLK↑ - LE	t_{H1}		9	-	-	ns
	GCLK – LE↓(vsync/swrst)	t_{H2}		300			ns
Propagation Delay Time	DCLK – SDO	t_{PD0}		-	24	25	ns
	GCLK – $\overline{OUT2n}$*	t_{PD1}		-	40		ns
	LE – SDO	t_{PD2}***		-	35	40-	ns
Pulse Width	LE	$t_{W(LE)}$		15			ns
Command to command		tcc		51	-	-	ns
Data Clock Frequency		F_{DCLK}		-	-	27	MHz
Gray Scale Clock Frequency		F_{GCLK}		-	-	26	MHz
Gray Scale Clock Frequency (The function of GCLK doubling is enabled)		F_{GCLK}		-	-	13	MHz
Min Clock(GCLK/DCLK) pulse width****		$t_{W(CLK)}$		13	-	-	Ns
Ratio of (GCLK freq)/(DCLK freq)		$R_{(GCLK/DCLK)}$		20	-	-	%
Compulsory error detection operation time***		t_{ERR-C}		700	-	-	ns
Output Rise Time of Output Ports		t_{OR}			20	30	ns
Output Fall Time of Output Ports		t_{OF}			20	30	ns
Dead time positive level		tdth		300			ns
Dead time negative level		tdtl		1200			ns

*Output waveforms have good uniformity among channels.

** Refer to the Timing Waveform, where n=0, 1, 2, 3, 4, 5, 6, 7.

***In timing of "configuration read", the next DCLK rising edge should be t_{PD2} after LE's falling edge.

****The Gray Scale Clock period must be 50% duty cycle when the function of GCLK multiplier is enabled.

*****Users have to leave more time than the maximum error detection time for the error detection.

Switching Characteristics (V_{DD}=3.3V, Ta=25°C)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Setup Time	SDI - DCLK↑	t_{SU0}	V_{DD}=3.3V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=1.4kΩ V_{DS}=1V R_L=300Ω C_L=10pF C_1=100nF C_2=10μF C_{SDO}=10pF V_{LED}=4.0V	7	-		ns
	LE – DCLK↑	t_{SU1}		10	-		ns
	LE↓(vsync/swrst) – GCLK	t_{SU2}		1200			ns
	LE↓ – DCLK↑	tsu3***		52			ns
Hold Time	DCLK↑ - SDI	t_{H0}		8	-		ns
	DCLK↑ - LE	t_{H1}		10	-		ns
	GCLK – LE↓(vsync/swrst)	t_{H2}		300			ns
Propagation Delay Time	DCLK – SDO	t_{PD0}		-	25		ns
	GCLK – $\overline{OUT2n}$*	t_{PD1}		-	45		ns
	LE – SDO	t_{PD2}***		-	40		ns
Pulse Width	LE	$t_{W(LE)}$		16			ns
Command to command		tcc		52	-	-	ns
Data Clock Frequency		F_{DCLK}		-	-	25	MHz
Gray Scale Clock Frequency		F_{GCLK}		-	-	20	MHz
Gray Scale Clock Frequency (The function of GCLK doubling is enabled)		F_{GCLK}		-	-	10	MHz
Min Clock(GCLK/DCLK) pulse width****		$t_{W(CLK)}$		13			Ns
Ratio of (GCLK freq)/(DCLK freq)		$R_{(GCLK/DCLK)}$		20		-	%
Compulsory error detection operation time***		t_{ERR-C}		700	-	-	ns
Output Rise Time of Output Ports		t_{OR}			25	35	ns
Output Fall Time of Output Ports		t_{OF}			25	35	ns
Dead time positive level		tdth		300			ns
Dead time negative level		tdtl		1200			ns

*Output waveforms have good uniformity among channels.

** Refer to the Timing Waveform, where n=0, 1, 2, 3, 4, 5, 6, 7.

***In timing of "configuration read", the next DCLK rising edge should be t_{PD2} after LE's falling edge.

****The Gray Scale Clock period must be 50% duty cycle when the function of GCLK multiplier is enabled.

*****Users have to leave more time than the maximum error detection time for the error detection.

Test Circuit for Switching Characteristics

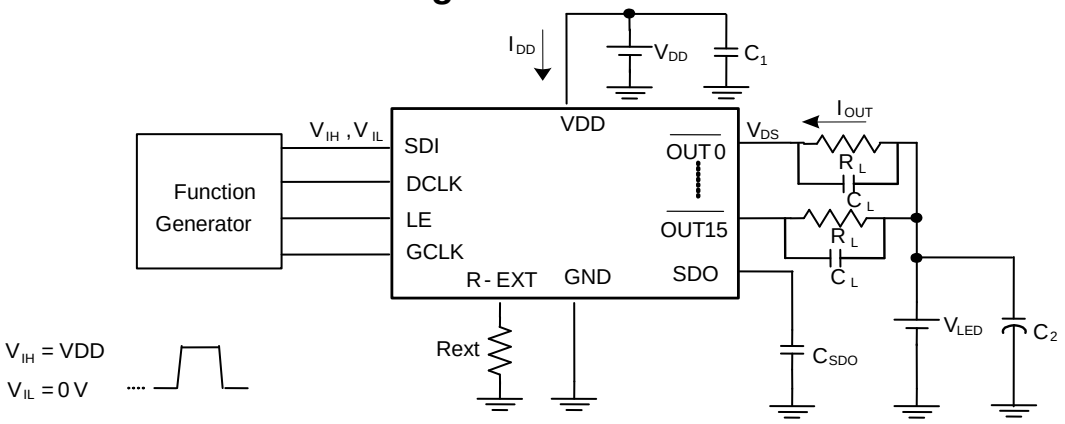
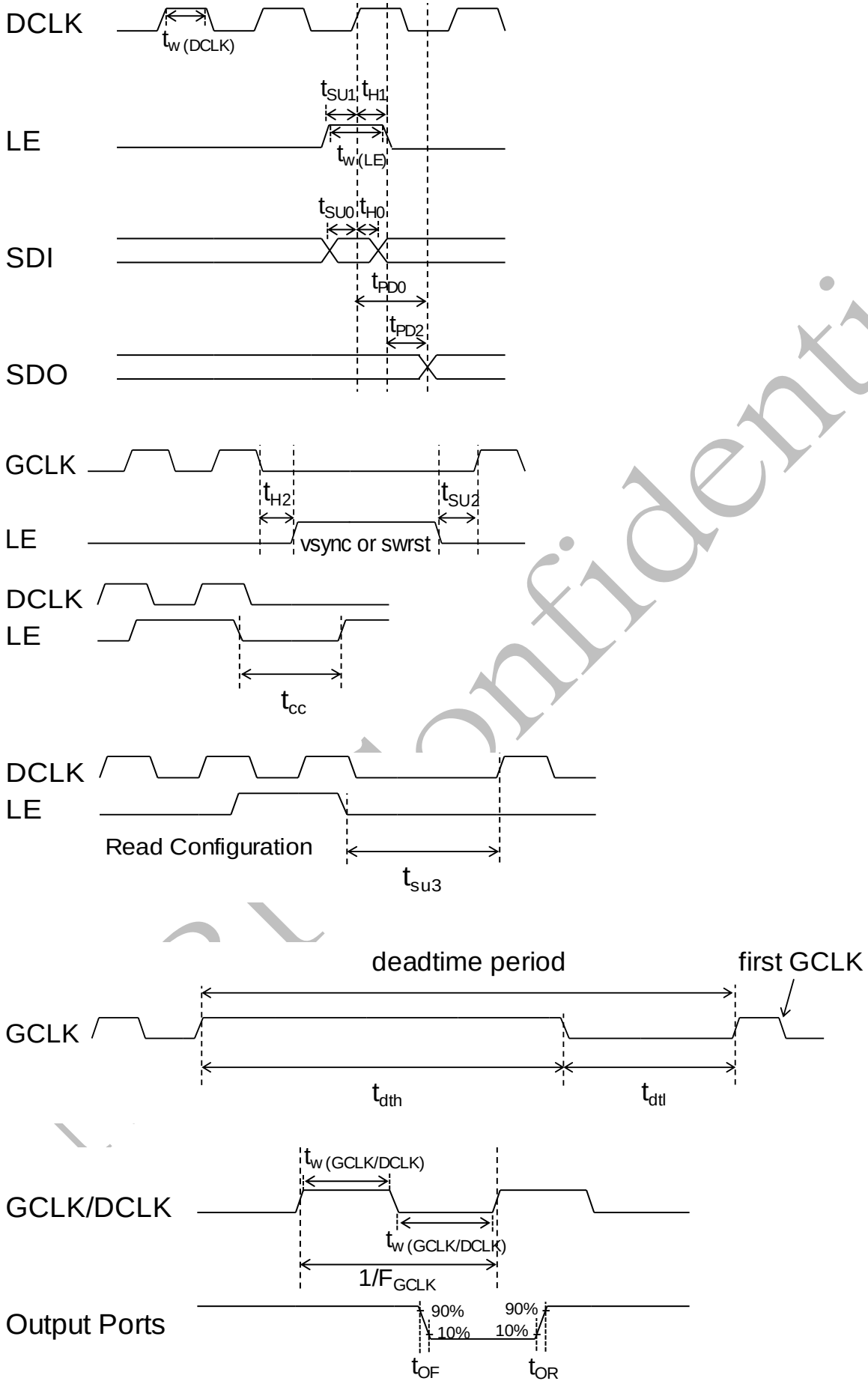


Figure 3

Timing Waveform



Control Command

Command Name	Signals Combination		Description
	LE	Number of DCLK Rising Edge when LE is asserted	The Action after a Falling Edge of LE
stop compulsory error detection	High	1	Stop compulsory error detection.
Individual Latch	High	1	Serial data are transferred to the buffers
Vertical Sync	High	2	Display frame will be updated
Write Configuration*	High	4	Serial data are transferred to the “configuration register”
Read Configuration	High	5	Serial data are transferred from the “configuration register”
Compulsory error detection(open error)	High	7	Start compulsory error detection(open error detection)
Write 2nd Configuration*	High	8	Serial data are transferred to the “2nd configuration register”
Read 2nd Configuration	High	9	Serial data are transferred from the “2nd configuration register”
Software reset	High	10	Reset all the digital part (not including configure registers)
Write 3rd Configuration*	High	16	Serial data are transferred to the “3rd configuration register”
Read 3rd Configuration	High	17	Serial data are transferred from the “3rd configuration register”
Write 4th Configuration*	High	18	Serial data are transferred to the “4th” configuration register”
Read 4th Configuration	High	19	Serial data are transferred from the “4th” configuration register”
Write 5th Configuration*	High	13	Serial data are transferred to the “5th” configuration register”
Read 5th Configuration	High	21	Serial data are transferred from the “5th” configuration register”
Write 6th Configuration*	High	15	Serial data are transferred to the “5th” configuration register”
Read 6th Configuration	High	22	Serial data are transferred from the “5th” configuration register”
HW reset	High	30	Force HW reset active

*Those commands can only be activated after Pre-Active command; otherwise, they will be invalid.

Note:

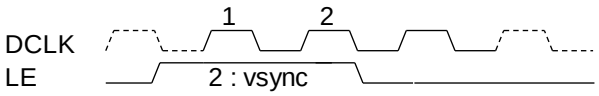
a.) Vsync cmd will be valid only after 16 individual latch cmds been sent at initial => for preventing power-on noise

b.) “Enable all outputs”, “Disable all outputs” and all test mode will be disabled after received “ind_le” cmd

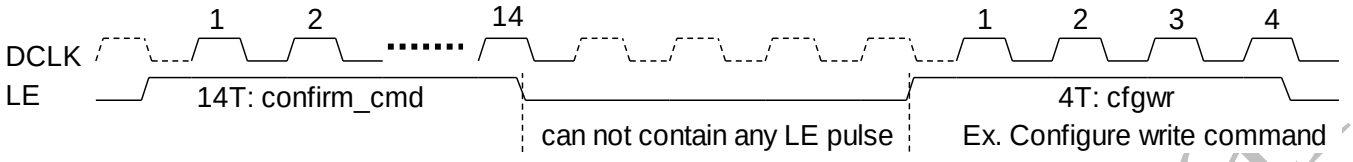
The following figure show the waveform spec. for commands which need or need not confirm-cmd ahead:.

Command which need no comfirm-command ahead

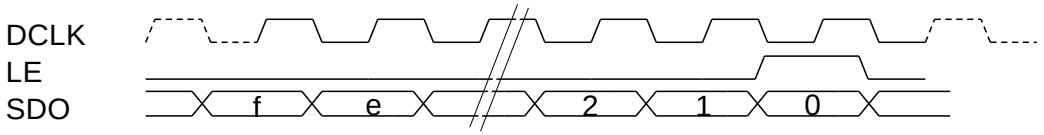
Command which need no comfirm-command ahead



Command which need comfirm-command ahead

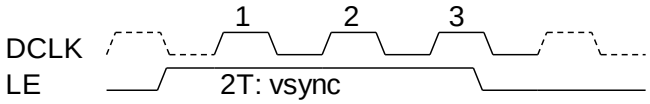


- Individual Latch



Note: GCLK can not stop during this command, and GCLK_freq / DCLK_freq >= 1/5

- Vertical Sync



Definition of 1st Configuration Register

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	0	0	1	1	1	1	1	1

Bit	Attribute	Definition	Value	Function
F~D	Read/Write	Reserve	000(default)	Reserve
C~8	Read/Write	Number of scan lines	00000 00001 00010 00011 (Default) ~ 11111	00000: 1 lines; 01000: 9 lines; 10000: 17 lines 00001: 2 lines; 01001: 10 lines; 10001: 18 lines 00010: 3 lines; 01010: 11 lines; 10010: 19 lines 00011: 4 lines; 01011: 12 lines …… 00100: 5 lines; 01100: 13 lines …… 00101: 6 lines; 01101: 14 lines; 11101: 30 lines 00110: 7 lines; 01110: 15 lines; 11110: 31 lines 00111: 8 lines; 01111: 16 lines; 11111: 32 lines
7	Read/Write	S-PWM mode	0 (Default)	The 16384 GCLKs(14-bit) PWM cycle is divided into 32 sections, each section has 512 GCLKs., User still send 16bit data with 2 bit 0 in LSB bits. Ex., {14'h1234, 2'h0}.
			1	The 8192 GCLKs(13-bit) PWM cycle is divided into 16 sections, each section has 512 GCLKs., User still send 16bit data with 3 bit 0 in LSB bits. Ex., {13'h1234, 3'h0}.
6	Read/Write	GCLK multiplier	0 (Default)	GCLK multiplier disable
			1	GCLK multiplier enable
5~0	Read/Write	Current Control	000,000 ~ 111,111(default)	[000,000] 12.5% ~ [111,111] 100%

Default setting of configuration register is 16'h033f

Definition of 2nd Configuration Register

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Attribute	Definition	Value	Function
F~B	Read/Write	Reserved	00(default)	Reserved
A	Read/Write	Double refresh	0(default)	(1) When 1st cfgreg[7] = 1'b0, the 16384 GCLK (14-bit) PWM cycle is divided into 32 sections, each section has 512 GCLK. (2) When 1st cfgreg[7] = 1'b1, the 8192 GCLK (13-bit) PWM cycle is divided into 16 sections, each section has 512 GCLK.
			1	(1) When 1st cfgreg[7] = 1'b0, the 16384 GCLK (14-bit) PWM cycle is divided into 64 sections, each section has 256 GCLK. (2) When 1st cfgreg[7] = 1'b1, the 8192 GCLK (13-bit) PWM cycle is divided into 32 sections, each section has 256 GCLK.
9	Read/Write	Reserved	0(default)	Reserved
8	Read/Write	Compensation of low gray 1	0(default)~11	0: Disable 1: Enable
7	Read/Write	Reserve	0(default)	Reserved
6~5	Read/Write	Compensation of low gray 2	00 (default) ~11	00~11: Low Level~High Level
4	Read/Write	Reserved	0	Reserved
3~1	Read/Write	Reserved	000 (default)	Reserved
0	Read/Write	Reserved	0(default)	Reserved

Default setting of configuration register is 16'h0000

Definition of 3th Configuration Register

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Attribute	Definition	Value	Function
15	Read/Write	Compensation of dark screen 1	0(default)	0:Disable 1:Enable
14~10	Read/Write	Compensation of dark screen 2	00000 ~ 11111(default)	Level setting when SDI=0 00001~11111: Low Level~High Level 00000 means disable
9~5	Read/Write	Compensation of dark screen 3	00000 ~ 11111(default)	Level setting when SDI=0 00001~11111: Low Level~High Level 00000 means disable
4~0	Read/Write	Compensation of dark screen 4	00000 ~ 11111(default)	Level setting when SDI=0 00001~11111: Low Level~High Level 00000 means disable

Default setting of configuration register is 16'h7fff

Definition of 4th Configuration Register

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Attribute	Definition	Value	Function
15	Read/Write	Compensation of displaying 1	0(default)	0:Dsable 1:Enable
14~10	Read/Write	Compensation of displaying 2	00000 ~ 11111(default)	Level setting when SDI=1 0,0001~1,1111: Low Level~High Level 00000 means disable
9~5	Read/Write	Compensation of displaying 3	00000 ~ 11111(default)	Level setting when SDI=1 0,0001~1,1111: Low Level~High Level 00000 means disable
4~0	Read/Write	Compensation of displaying 4	00000 ~ 11111(default)	Level setting when SDI=1 0,0001~1,1111: Low Level~High Level 00000 means disable

Default setting of configuration register is 16'h7fff

Definition of 5th Configuration Register

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

Bit	Attribute	Definition	Value	Function
F	Read/Write	Config reg6 enable	0(Default)	1: Enable 0: Disable
E	Read/Write	Reserve	0(Default)	Reserve
D	Read/Write	Reserve	0(default)	Reserve
C	Read/Write	Reserve	0(default)	Reserve
B~8	Read/Write	Reserve	00(default)~11	Reserve
7~5	Read/Write	Open Error detection level select	000(default)~111	[000]~[111]: Low level~High level
4~0	Read/Write	Precharge	00000 ~ 11111(default)	00001~11111: Low Level~High Level 00000 means disable during deadtime

Default setting of configuration register is 16'h001f

Definition of 6nd Configuration Register

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Attribute	Definition	Value	Function
F~0	Read/Write	Reserve	0(Default)	Reserve

Default setting of configuration register is 16'h0000

Number of Scan Line

MBI5253 supports 1 to 32 scan lines. Please set the configuration register1 bit [C:8] according to the application. The default value '00011' is 4 scan lines.

Gray Scale Mode and Scan-type S-PWM

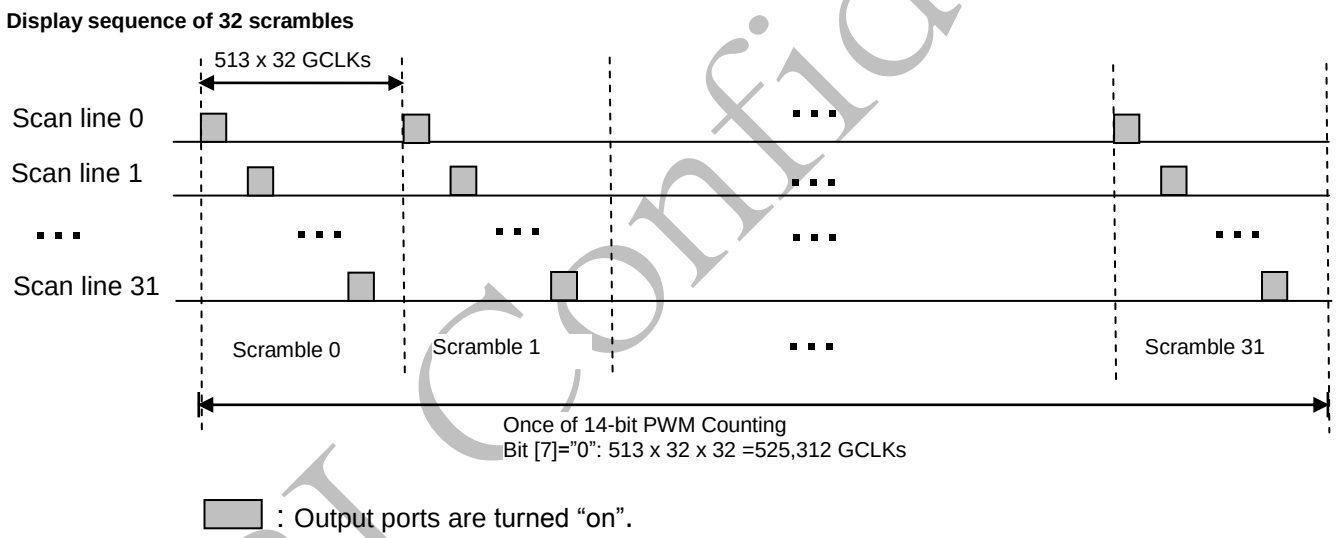
MBI5253 provides a selectable 14-bit or 13-bit gray scale by setting the configuration register1 bit [7]. The default value is set to '0' for 14-bit color depth. In 14-bit gray scale mode, users should still send 16-bit data with 2-bit '0' in LSB bits. For example, {14'h1234, 2'h0}.

MBI5253 has a smart S-PWM technology for scan type. With S-PWM, the total PWM cycles can be broken into MSB (Most Significant Bits) and LSB (Least Significant Bits) of gray scale cycles. The MSB information can be broken down into many refresh cycles to achieve overall same high bit resolution.

GCLK multiplier

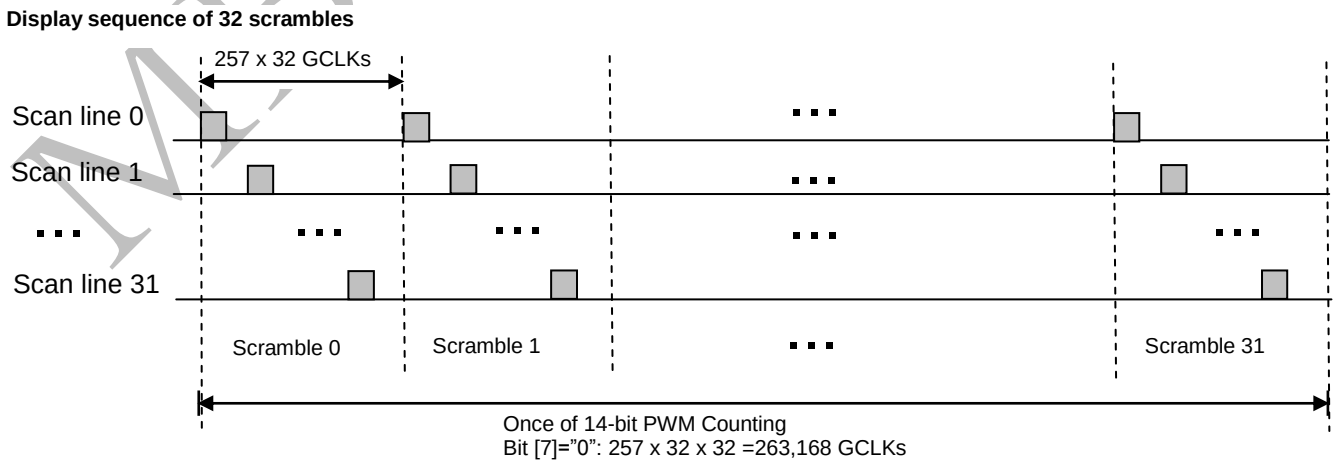
MBI5253 provides a GCLK multiplier function by setting the configuration register1 bit [6]. The default value is set to '0' for GCLK multiplier disable.

GCLK multiplier disabled (configuration register1 bit [6] = 0)



: Output ports are turned "on".

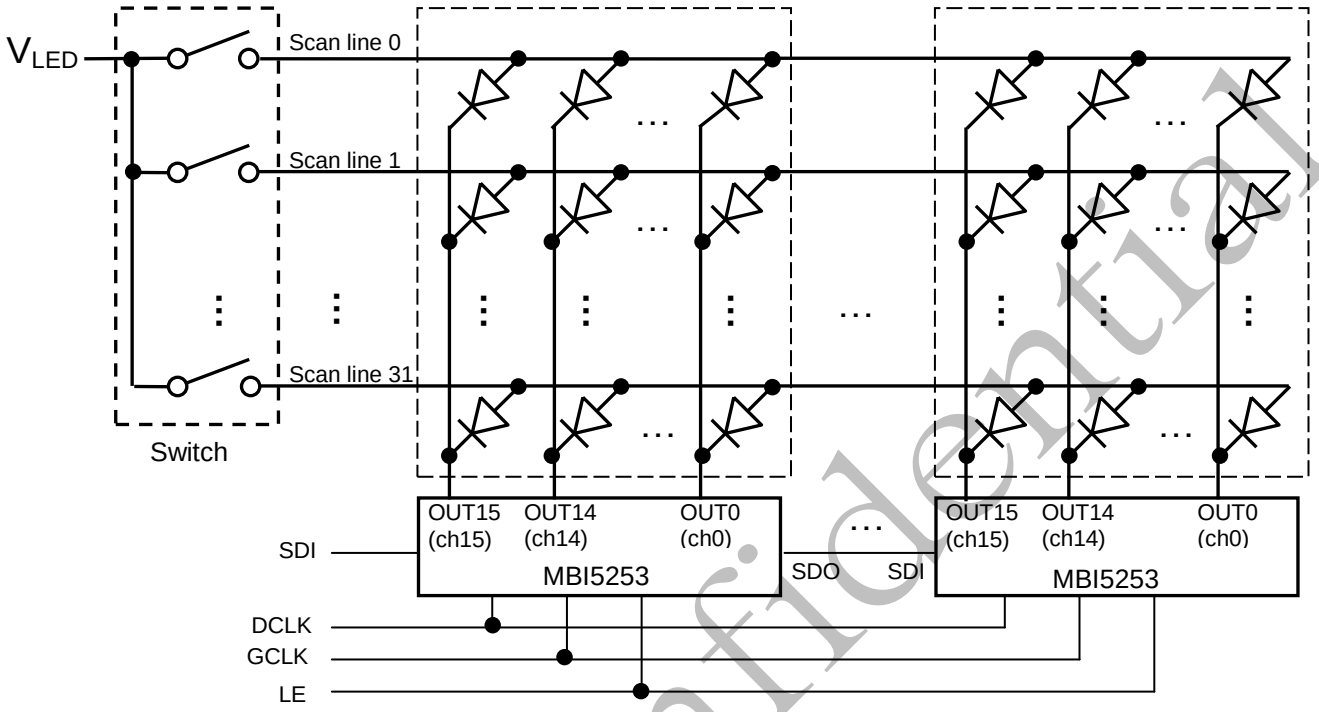
GCLK multiplier enabled (configuration register1 bit [6] = 1)



: Output ports are turned "on".

Operation Principal

Scan type application structure



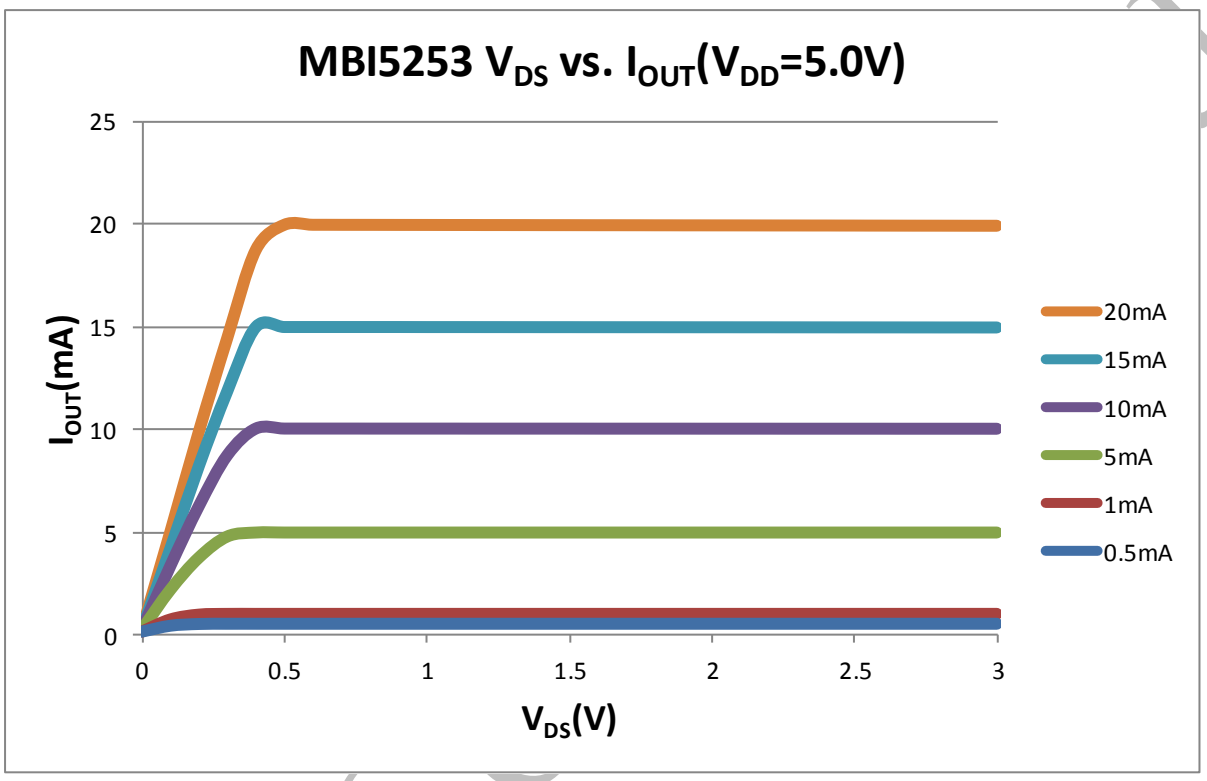
The above figure shows the suggested application structure of scan type scheme with 32 scan lines. The gray-scale data are sent by pin "SDI and SDO" with the commands formed by pin "LE" and "DCLK". The output ports from 16 channels ($\overline{OUT0}$ ~ $\overline{OUT15}$) will output the PWM result for each scan line at different time, so there must be one "Switch" to multiplex for each scan line. The switching sequence and method and the command usage will be described in the application note.

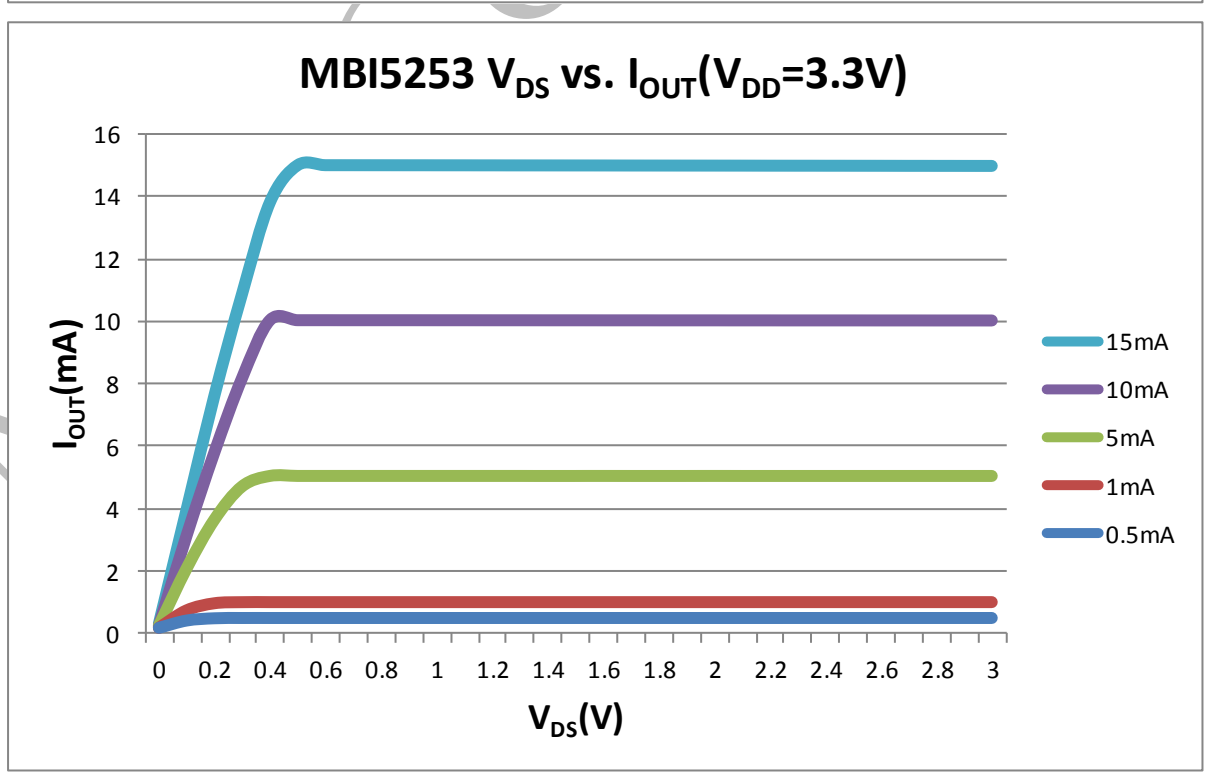
Constant Current

In LED display application, MBI5253 provides nearly no variation in current from channel to channel and from IC to IC. This can be achieved by:

1) The maximum current variation between channels is less than 2.5%, and that between ICs is less than ±3%

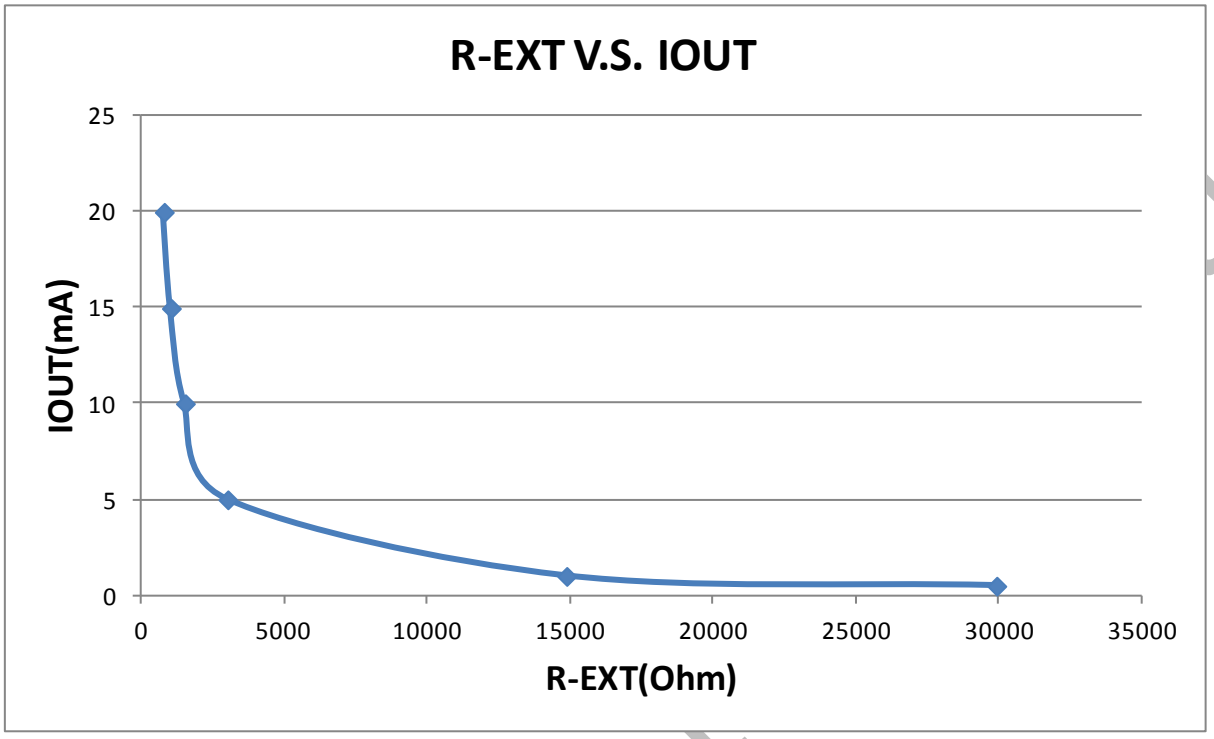
2) In addition, the current characteristic of output stage is flat and user can refer to the figure below. The output current can be kept constant regardless of the variations of LED forward voltages (V_F). This guarantees LED to be performed on the same brightness as user's specification.





Setting Output Current

The output current (I_{OUT}) is set by an external resistor, R_{ext}. The default relationship between I_{OUT} and R_{ext} is shown in the following figure.

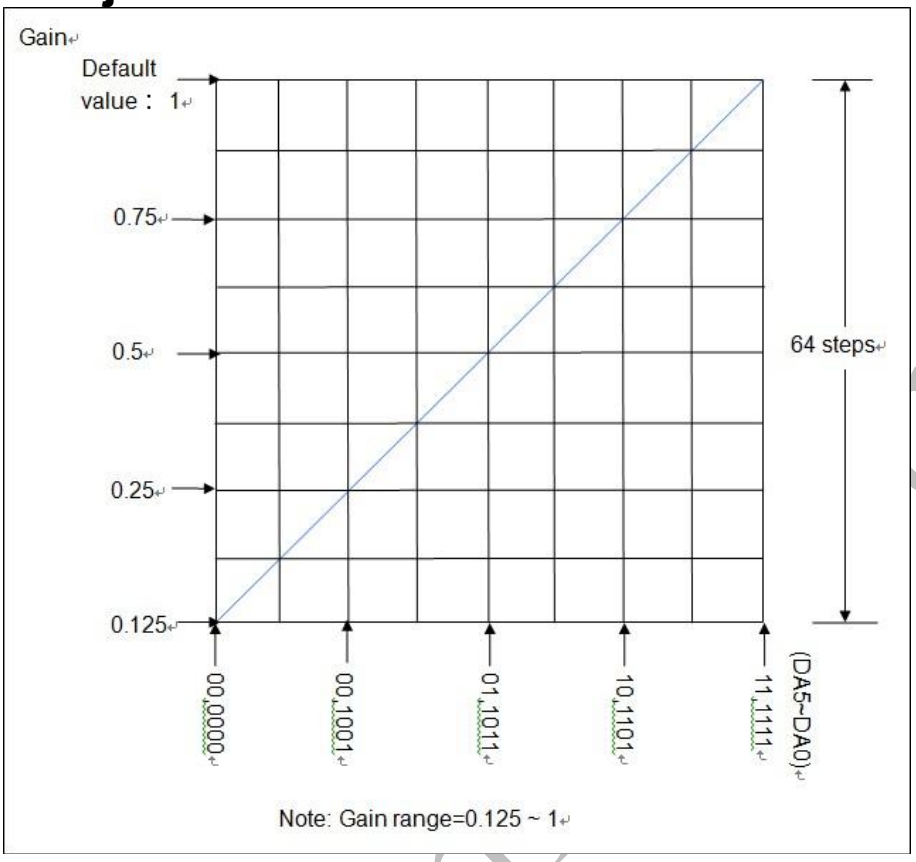


Also, the output current can be calculated from the equation:

$V_{R\text{-}EXT}$=0.61Volt x G; I_{OUT}= ($V_{R\text{-}EXT}/R_{ext}$) x24xG

Whereas R_{ext} is the resistance of the external resistor connected to R-EXT terminal and $V_{R\text{-}EXT}$ is its voltage. G is the digital current gain, which is set by the bit5 – bit0 of the configuration register. The default value of G is 1. The formula and setting for G are described in next section.

Current Gain Adjustment



The 6 bits (bit 5~bit 0) of the configuration register set the gain of output current, i.e., G. As total 6-bit in number,
i.e., ranged from 6'b000000 to 6'b111111, these bits allow the user to set the output current gain up to 64 levels.
These bits can be further defined inside configuration register as follows:

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	DA5	DA4	DA3	DA2	DA1	DA0

Bit 5 to bit 0 are DA5 ~ DA0.
The relationship between these bits and current gain G is:
G=0.125+(D/63)x0.875
and D in the above decimal numeration can be converted to its equivalent in binary form by the following equation:
$D= DA5x2^5+DA4x2^4+DA3x2^3+DA2x2^2+DA1x2^1+DA0x2^0$
In other words, these bits can be looked as 6-bit mantissa DA5~DA0.
For example,
G=0.5, D=(0.5-0.125)/0.875x63=27
the D in binary form would be:
$D=27=0x2^5+1x2^4+1x2^3+0x2^2+1x2^1+1x2^0$
The 6 bits (bit 5~bit 0) of the configuration register are set to 6'b011011

Package Power Dissipation (PD)

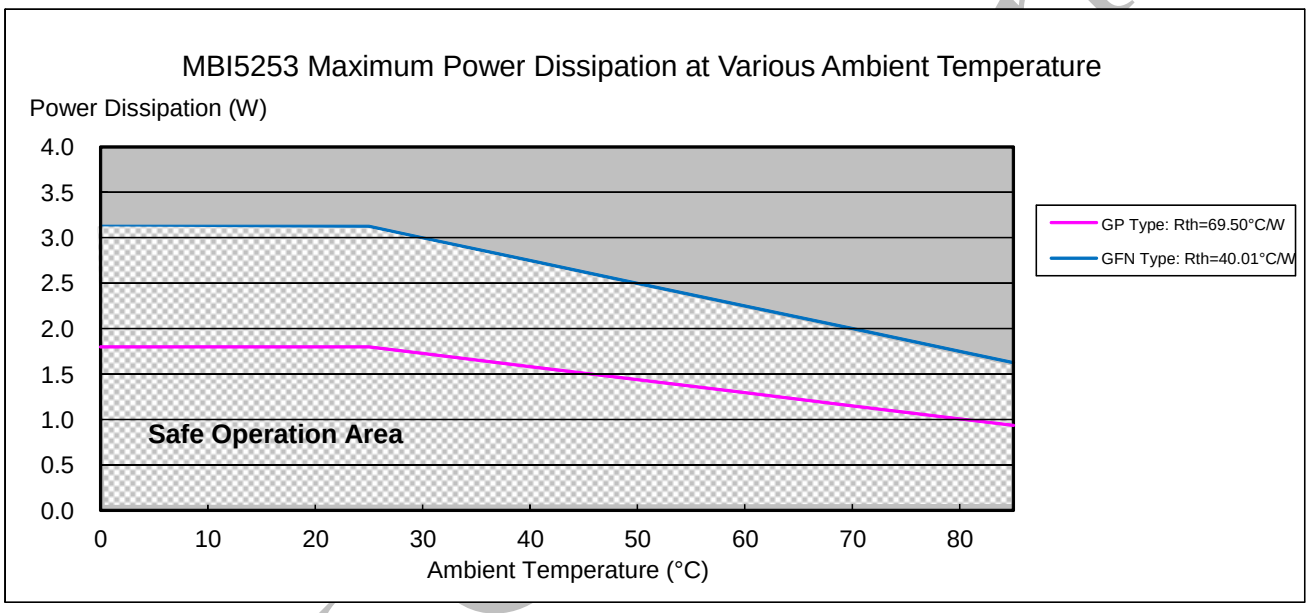
The maximum allowable package power dissipation is determined as $P_D(max)=(Tj–Ta)/R_{th(j-a)}$. When 16 output channels are turned on simultaneously, the actual package power dissipation is $P_D(act)=(I_{DD}xV_{DD})+(I_{OUT}xDutyxV_{DS}x16)$. Therefore, to keep $P_D(act)\leq P_D(max)$, the allowable maximum output current as a function of duty cycle is:

$I_{OUT}=\{[(Tj–Ta)/R_{th(j-a)}]–(I_{DD}xV_{DD})\}/V_{DS}/Duty/16$, where Tj=150°C.

Please see the follow table for P_D and $R_{th(j-a)}$ for different packages:

Device Type	$R_{th(j-a)}$ (°C/W)	P_D (W)
GP	69.50	1.79
GFN	40.01	3.12

The maximum power dissipation, $P_D(max)=(Tj–Ta)/R_{th(j-a)}$, decreases as the ambient temperature increases.



LED Supply Voltage (V_{LED})

MBI5253 is designed to operate with V_{DS} ranging from 0.4V to 1.0V (depending on I_{OUT}=1~20mA) considering the package power dissipating limits. V_{DS} may be higher enough to make $P_{D\ (act)} > P_{D\ (max)}$ when V_{LED}=5V and $V_{DS}=V_{LED}-V_F$, in which V_{LED} is the load supply voltage. In this case, it is recommended to use the lowest possible supply voltage or to set an external voltage reducer, V_{DROP}.

A voltage reducer lets $V_{DS}=(V_{LED}-V_F)-V_{DROP}$.

Resistors or Zener diode can be used in the applications as shown in the following figures.

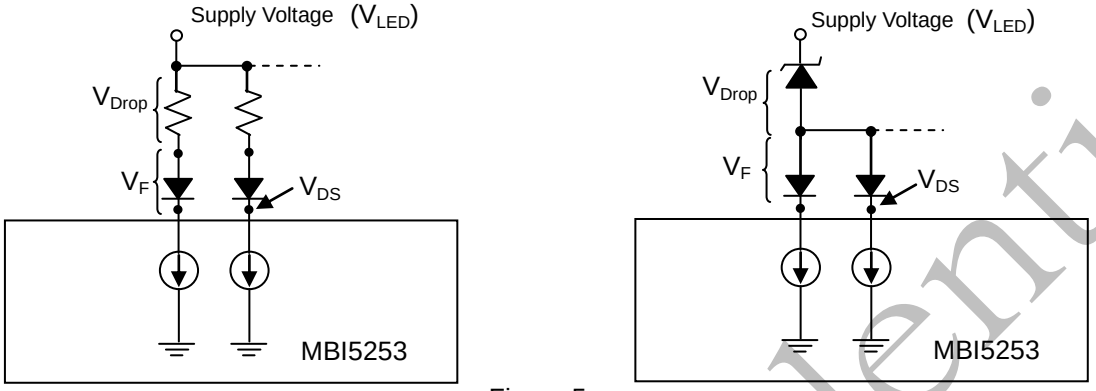


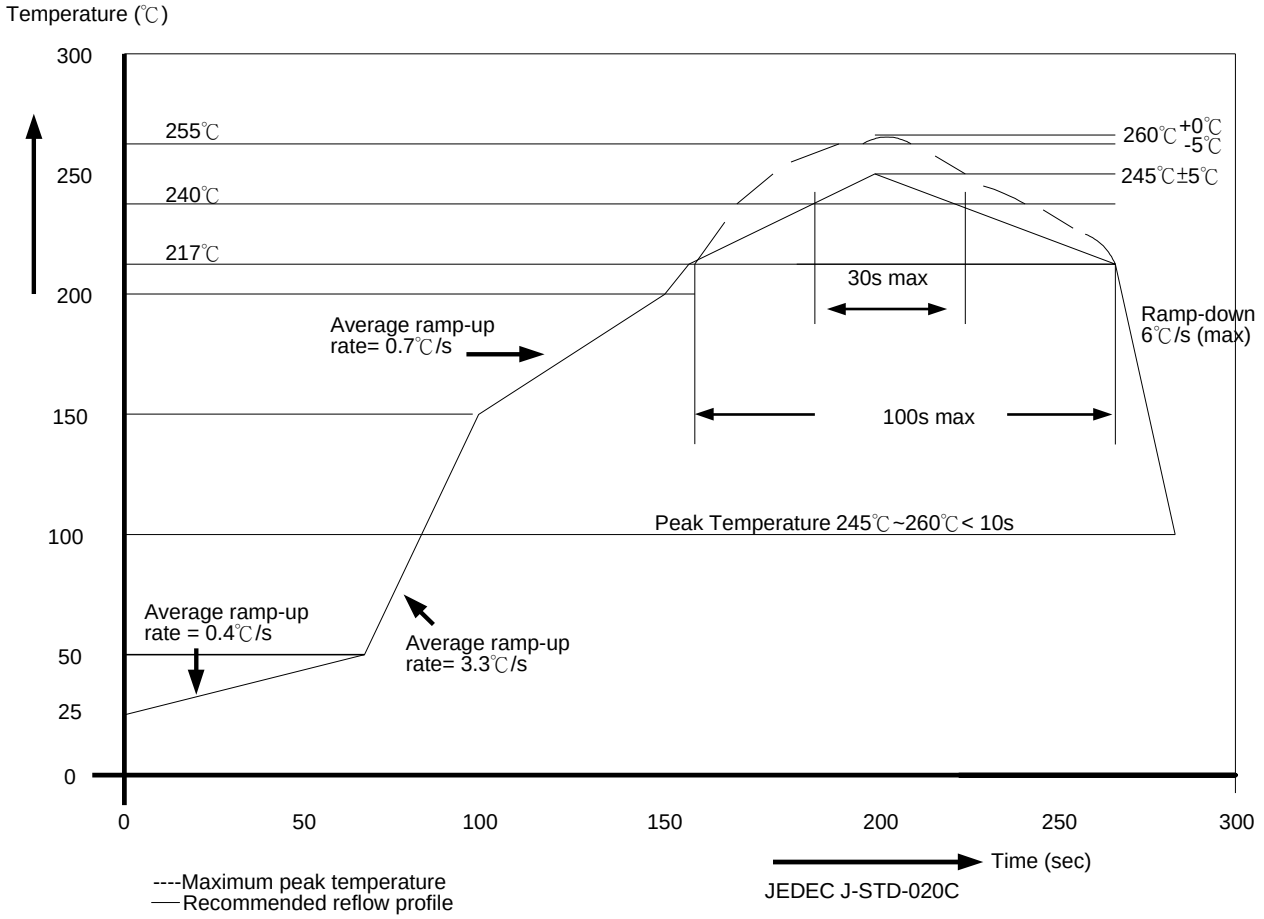
Figure 5

Switching Noise Reduction

LED drivers are frequently used in switch-mode applications which always behave with switching noise due to the parasitic inductance on PCB. To eliminate switching noise, refer to “Application Note for 8-bit and 16-bit LED Drivers- Overshoot”.

Soldering Process of "Pb-free & Green" Package Plating*

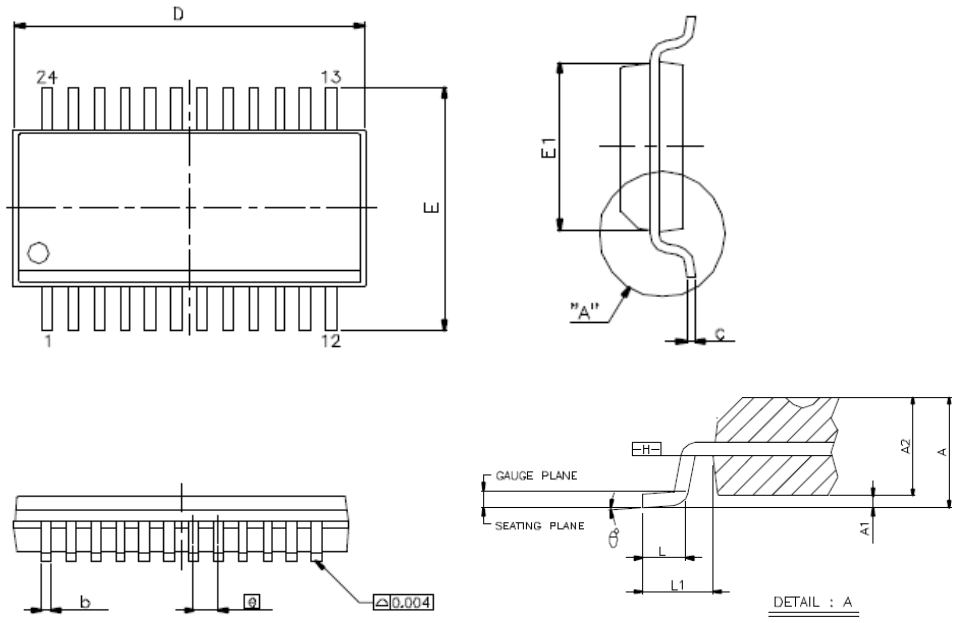
Macroblock has defined "Pb-Free & Green" to mean semiconductor products that are compatible with the current RoHS requirements and selected 100% pure tin (Sn) to provide forward and backward compatibility with both the current industry-standard SnPb-based soldering processes and higher-temperature Pb-free processes. Pure tin is widely accepted by customers and suppliers of electronic devices in Europe, Asia and the US as the lead-free surface finish of choice to replace tin-lead. Also, it adopts tin/lead (SnPb) solder paste, and please refer to the JEDEC J-STD-020C for the temperature of solder bath. However, in the whole Pb-free soldering processes and materials, 100% pure tin (Sn) will all require from 245 °C to 260°C for proper soldering on boards, referring to JEDEC J-STD-020C as shown below. .



Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 ≧2000
<1.6mm	260 +0 °C	260 +0 °C	260 +0 °C
1.6mm – 2.5mm	260 +0 °C	250 +0 °C	245 +0 °C
≧2.5mm	250 +0 °C	245 +0 °C	245 +0 °C

*Note: For details, please refer to Macroblock's "Policy on Pb-free & Green Package".

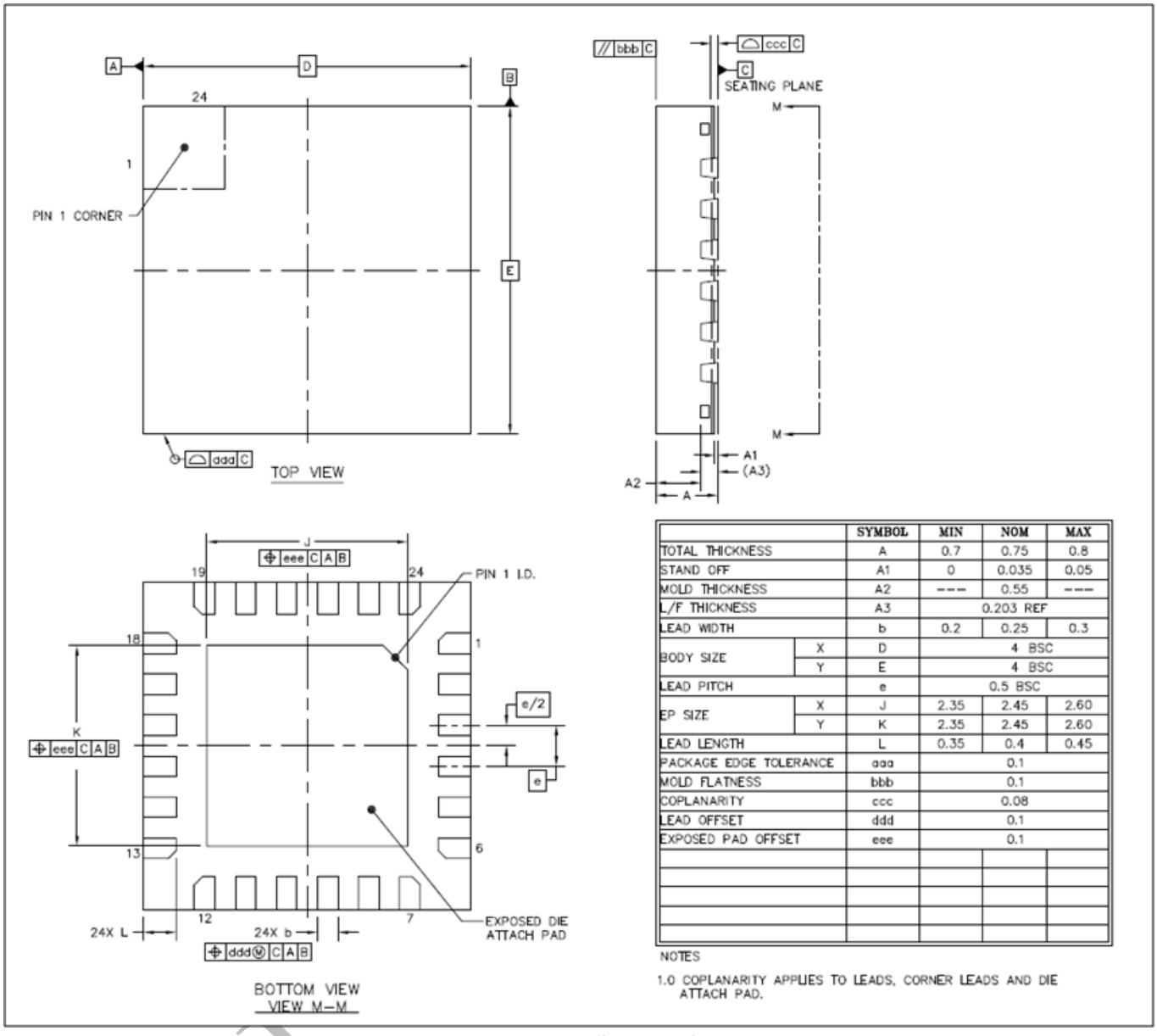
Package Outline



SYMBOLS	Dimensions shown in inchs			Dimensions shown in millimeters		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.053	0.064	0.069	1.346	1.626	1.753
A1	0.004	0.006	0.010	0.102	0.152	0.254
A2	—	—	0.059	—	—	1.499
D	0.337	0.341	0.344	8.560	8.661	8.738
E	0.228	0.236	0.244	5.791	5.994	6.198
E1	0.150	0.154	0.157	3.810	3.912	3.988
b	0.008	—	0.012	0.203	—	0.305
c	0.007	—	0.010	0.178	—	0.254
L	0.016	0.025	0.050	0.406	0.635	1.270
e	0.025 BASIC			0.635 BASIC		
L1	0.041 BASIC			1.0414 BASIC		
θ°	0	—	8	0	—	8

MBI5253 GP Outline Drawing

Note: The unit of the outline drawing is millimeter (mm).



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	2.35	2.45	2.60
	Y	K	2.35	2.45	2.60
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

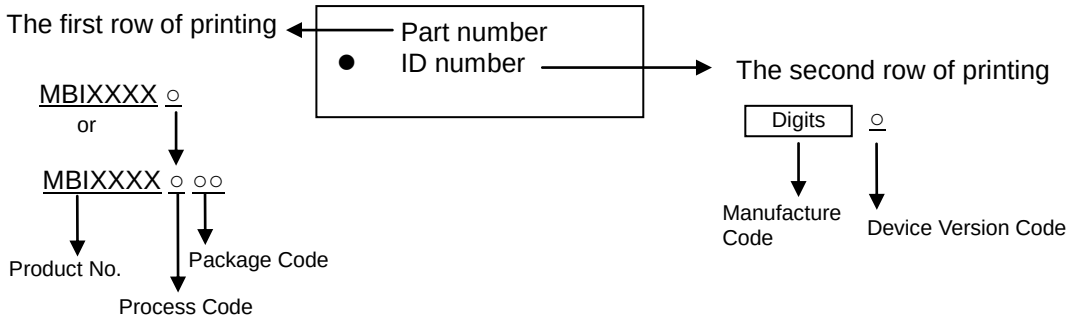
NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

MBI5253GFN Outline Drawing

Note: The unit of the outline drawing is millimeter (mm).

Product Top Mark Information



Product Revision History

Datasheet Version	Devise Version Code
V0.01	T
V0.02	T
V0.03	T
V0.04	T

Product Ordering Information

Product Ordering Number*	RoHS Compliant Package Type	Weight (g)
MBI5253GP-A	SSOP24L-150-0.64	0.11
MBI5253GFN-A	QFN24L-4*4-0.5	0.0379

*Please place your order with the ***"product ordering number"*** information on your purchase order (PO).

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